IN THE CLAIMS:

Amend claim 70, as follows:

70. (Amended) A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, [and a controller connectable to said processor for controlling operation of the array,] comprising:

providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,

identifying when a sector becomes defective,

storing an address of the defective sector in a sector defect map,

linking with the defective sector address in the defect map an address of another sector that is not defective, and

accessing a sector of the memory system by, when the sector being accessed is defective, referring to the sector defect map to translate the address of the defective sector being accessed into an address of another sector that is not defective, thereby to remap the defective sector into another sector that is not ~~defective~~.

Add the following new claims:

--76. The method according to claim 70, additionally comprising storing in individual ones of said sectors both user data and overhead information related to either the accessed usable sector or the user data stored therein.--

--77. The method according to claim 76, wherein the storing of overhead information includes storing sector addresses in the individual sectors that are related to the addresses of the individual sectors in which they are stored.--

--78. The method according to claim 76, wherein the storing of overhead information includes storing in the individual sectors error correction codes for user data stored in corresponding individual sectors.--

--79. A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, comprising:

providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,

partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion,

detecting a predefined condition when individual sectors become unusable and adding addresses of such unusable sectors to a list maintained within the card that links such unusable sector addresses with addresses of other sectors that are useable,

causing the controller, in response to receipt from the processor of an address in a format designating at least one magnetic disk sector, to generate an address of a non-volatile memory sector that corresponds to said at least one magnetic disk sector,

accessing a usable sector of the memory system, if the sector with the generated address is unusable, by referring to the list to translate the unusable sector address into an address of another sector that is usable and then accessing that other sector,

either writing data to, or reading data from, the user data portion of the accessed usable sector, and

either writing to, or reading from, said overhead portion of the accessed usable sector, information related to either the accessed usable sector or data stored in the user data portion of

~~said accessed useful sector.~~

--~~80~~ 2. The method according to claim ~~79~~ 1, wherein the detecting of the predefined condition includes detecting when individual sectors become defective.--

--~~81~~ 3. The method according to claim ~~80~~ 2, wherein the detecting of when individual sectors become defective includes determining when a number of individual defective memory cells within a sector exceed a given number.--

--~~82~~ 4. The method according to claim ~~79~~ 1, wherein the user data portion of the individual non-volatile memory sectors has a capacity of substantially 512 bytes.--

--~~83~~ 5. The method according to claim ~~79~~ 1, wherein the information stored in the overhead portion of the individual sectors includes an address of the respective ones of the individual sectors.--

--84. The method according to claim 79, wherein the information stored in the overhead portion of the individual sectors includes an error correction code for data stored in the user data portions of corresponding ones of the individual sectors.--

--~~85~~ 10. A method of operating a computer system including a processor and a memory system, wherein the memory system includes an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said array of memory cells that are erasable together as a unit, comprising:

providing said memory array and a memory controller within a card that is removably connectable to the computer system, said controller being connectable to said processor for controlling operation of the array when the card is connected to the computer system,

partitioning the memory cells within the individual sectors into at least a user data portion and an overhead portion,

causing the controller, in response to receipt from the processor of an address in a format designating at least one

magnetic disk sector, to designate an address of at least one non-volatile memory sector that corresponds with said at least one magnetic disk sector,

either writing user data to, or reading user data from, the user data portion of said at least one non-volatile memory sector, and

either writing to, or reading from, said overhead portion of said at least one non-volatile memory sector, overhead data related either to said at least one non-volatile memory sector or to data stored in the user data portion of said at least one non-volatile memory sector.--

--~~86~~ 11. The method of claim ~~85~~ 16, wherein the user data portion of the individual sectors has a capacity of substantially 512 bytes.--

--~~87~~ 12. The method of claim ~~85~~ 10, wherein the overhead data stored in said overhead portion of the individual sectors includes addresses of the individual sectors.--

--88. The method of claim 85, wherein the partitioning step includes partitioning the memory cells within the individual sectors to include an additional portion of spare memory cells.--

--~~89~~ 14. The method of claim ~~88~~ 13, wherein the overhead data stored in said overhead portion of the individual sectors includes an identification of any defective cells within the user data portion of corresponding ones of said sectors, said method additionally comprising causing the controller to read the identification of defective cells from the overhead portion of said addressed at least one non-volatile memory sector and then to substitute therefore other cells within the spare cell portion of the addressed at least one non-volatile memory sector.--

--90. The method of claim 85, additionally comprising causing the controller to identify and store addresses of any defective non-volatile memory sectors within the array, and, wherein the sector addressing step includes, in response to designating an address of a defective sector, substituting an address of another sector instead.--

--~~91~~ 16. The method of claim ~~85~~ 10, wherein the individual sectors include only one user data portion and only one overhead data portion.--

--92. A memory system on a card that is connectable to a host computer system, said memory system comprising:

an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said memory cells that are erasable together as a unit, the individual sectors having enough cells for storing a given amount of user data and overhead data, and

means connectable to said computer system for controlling operation of the array, said controlling means including:

means responsive to receipt of a magnetic disk sector address from the host computer system for addressing a corresponding non-volatile memory sector,

means for reading the overhead data stored in the addressed sector, and

means responsive to the read overhead data for executing an instruction from the host computer system to perform a designated one of reading user data from, ~~writing user data to or erasing the addressed sector.~~--

--~~93~~ 18. The memory system according to claim ~~92~~ 17 wherein said controlling means additionally includes means listing any unusable ones of said plurality of non-volatile memory sectors for linking said unusable sectors with others of said sectors that are usable, and wherein said non-volatile memory sector addressing means includes means for accessing linked others of said sectors in place of said unusable sectors.--

--~~94~~ 19. The memory system according to claim ~~92~~ 17 wherein said given amount of user data is substantially 512 bytes.--

--95. The memory system according to ~~claim~~ 82 wherein said magnetic disk sector address includes a head, cylinder and sector.--

--96. The memory system according to claim 82 wherein the individual sectors of the memory array additionally have enough